

ABSTRACT:

A PARALLEL COUNTER AND A LOGIC CIRCUIT FOR PERFORMING MULTIPLICATION

A logic circuit such as a parallel counter comprises logic for generating output bits as elementary symmetric functions of the input bits. The parallel counter can be used in a multiplication circuit. A multiplication circuit is also provided in which an array of combinations of each bit of a binary number with each other bit of another binary number is generated having a reduced form in order to reduce the steps required in array reduction.

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